FIG. 1
(PRIOR ART)

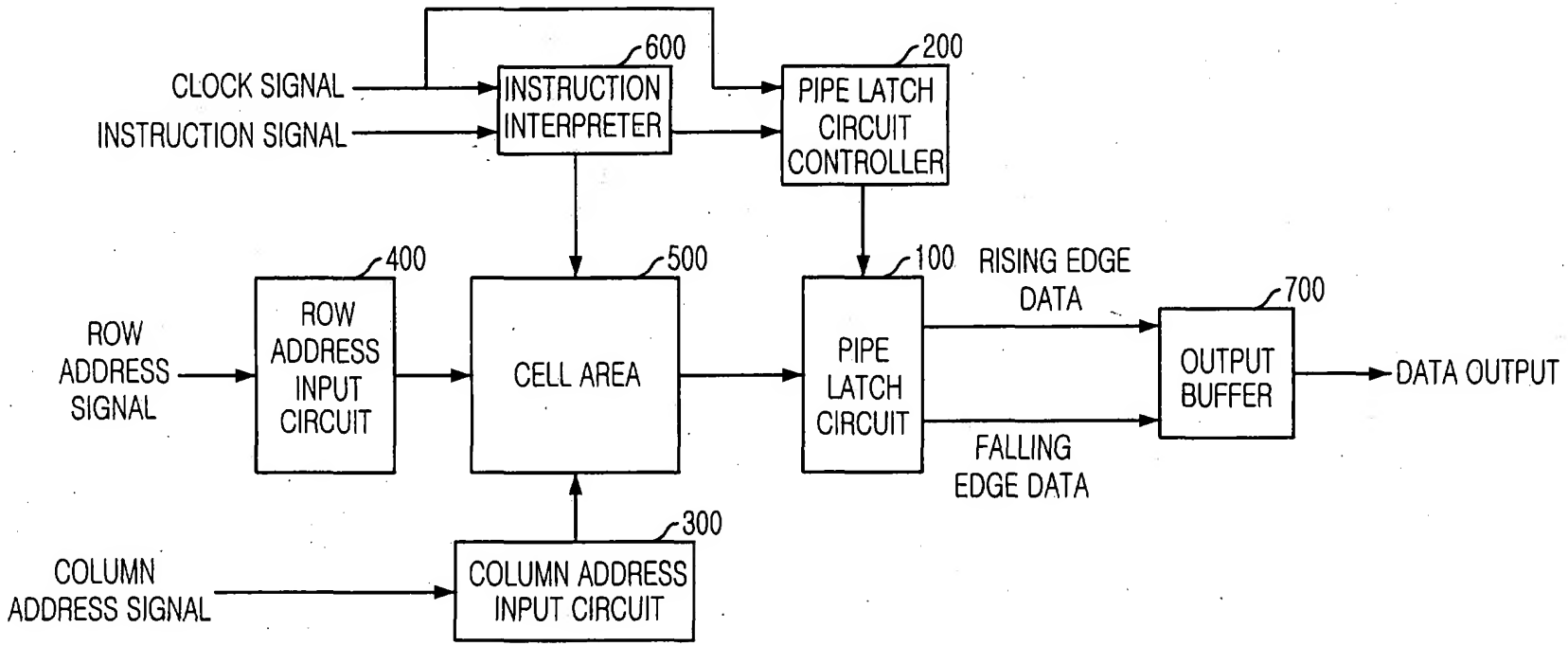


FIG. 2A
(PRIOR ART)

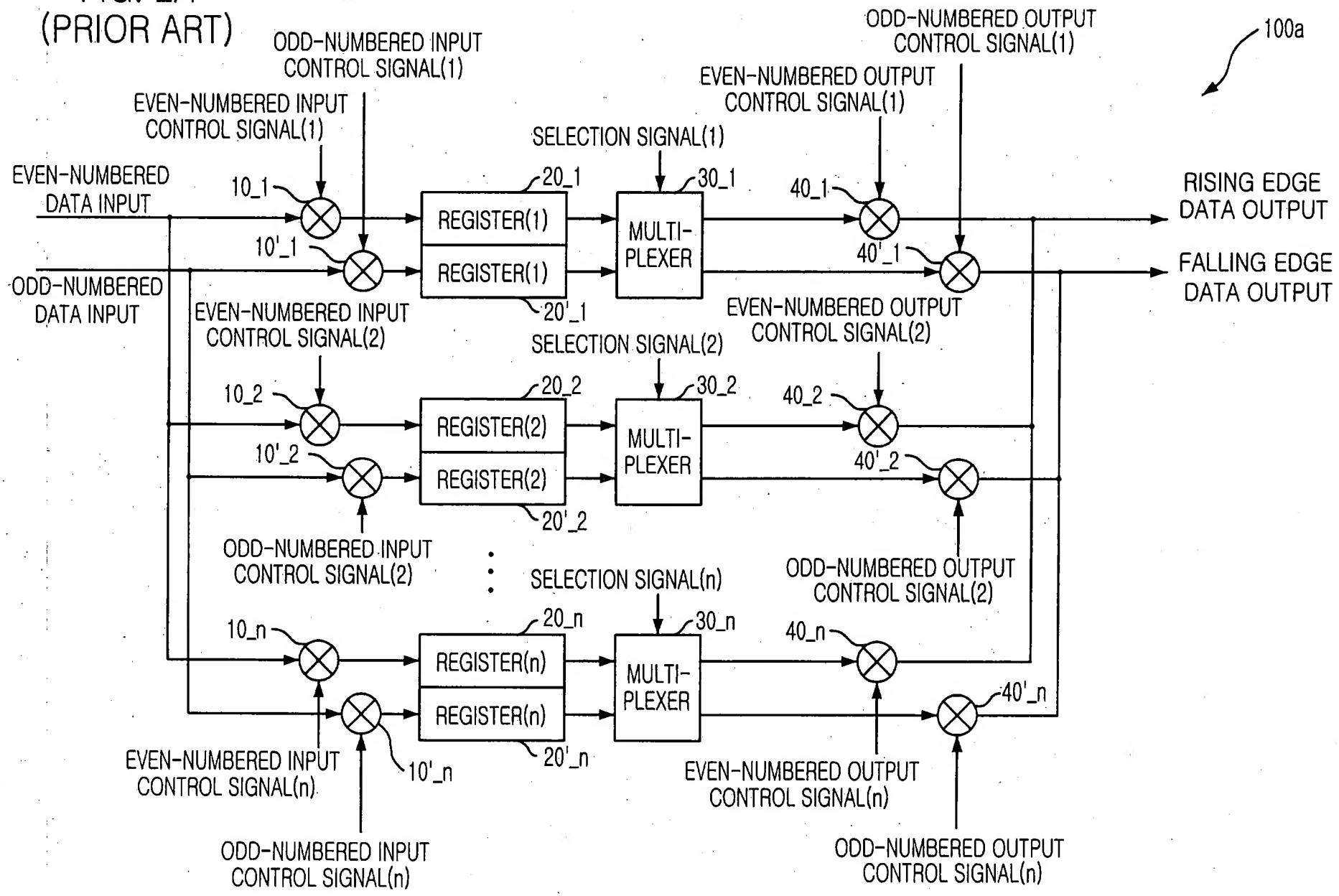


FIG. 2B
(PRIOR ART)

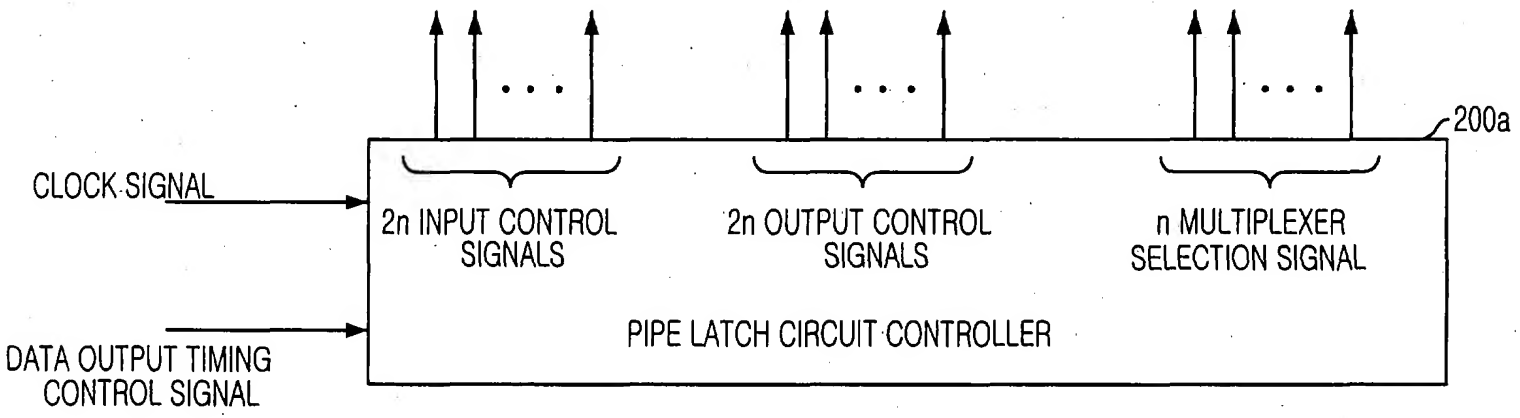


FIG. 3
(PRIOR ART)

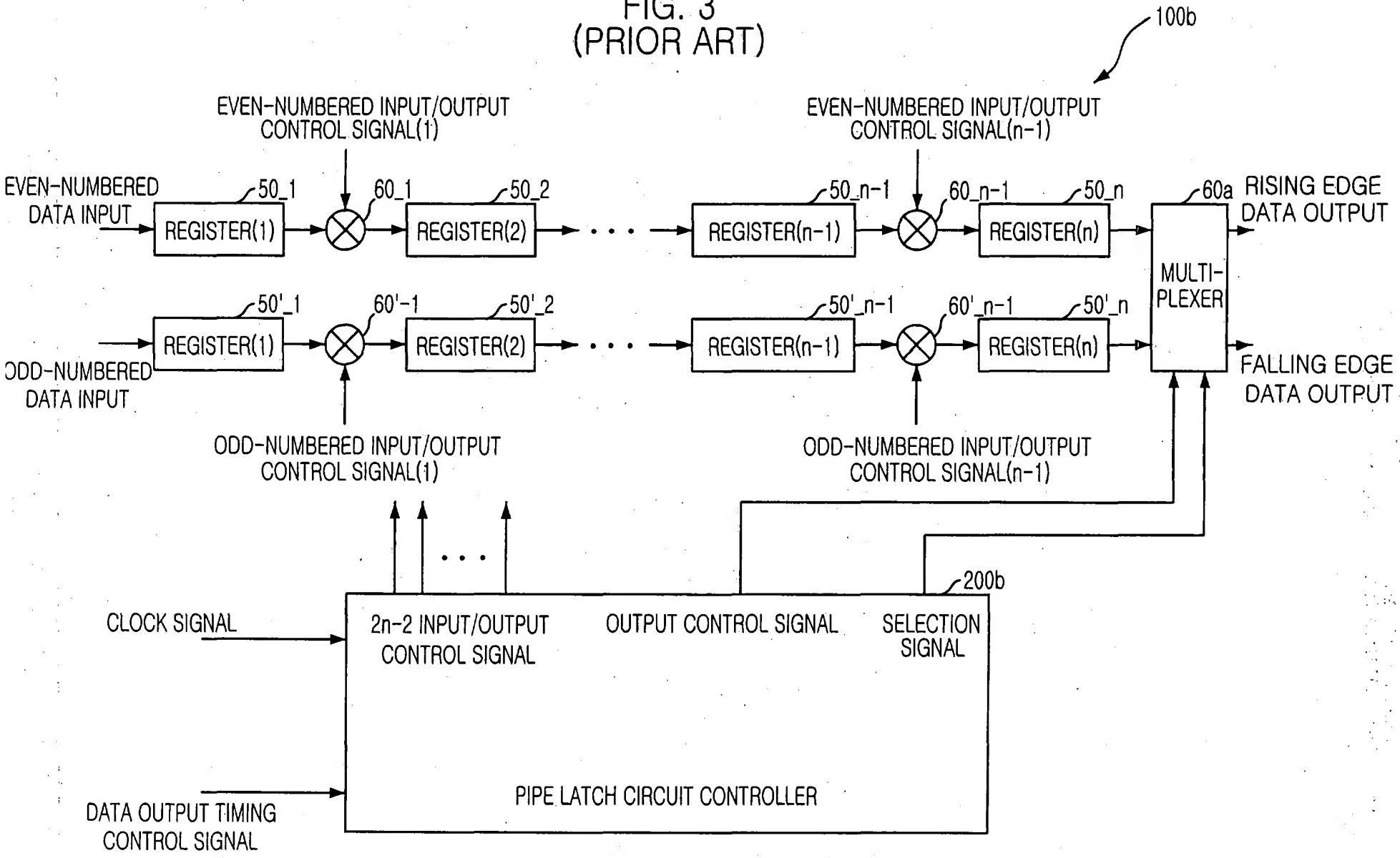


FIG. 4

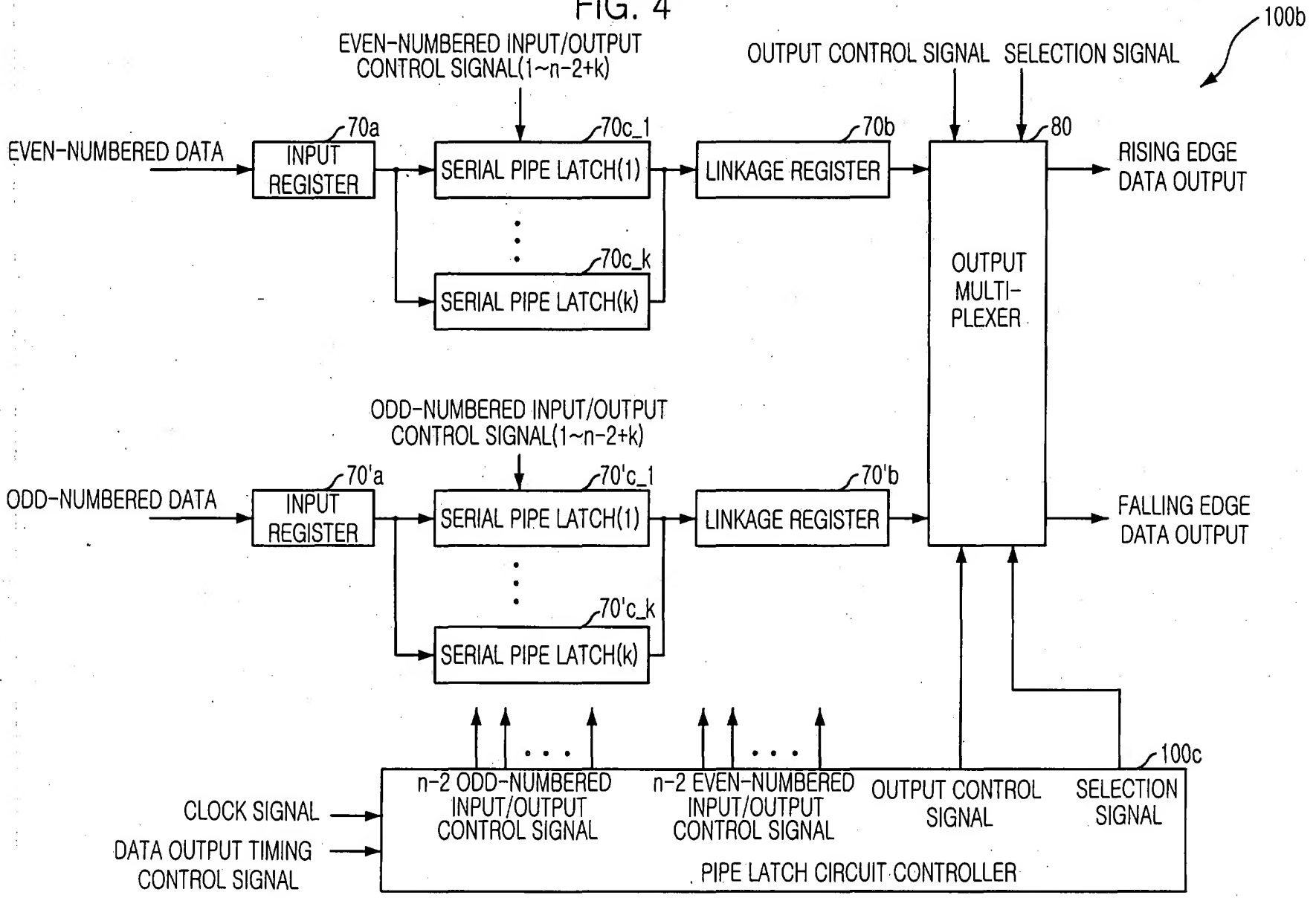
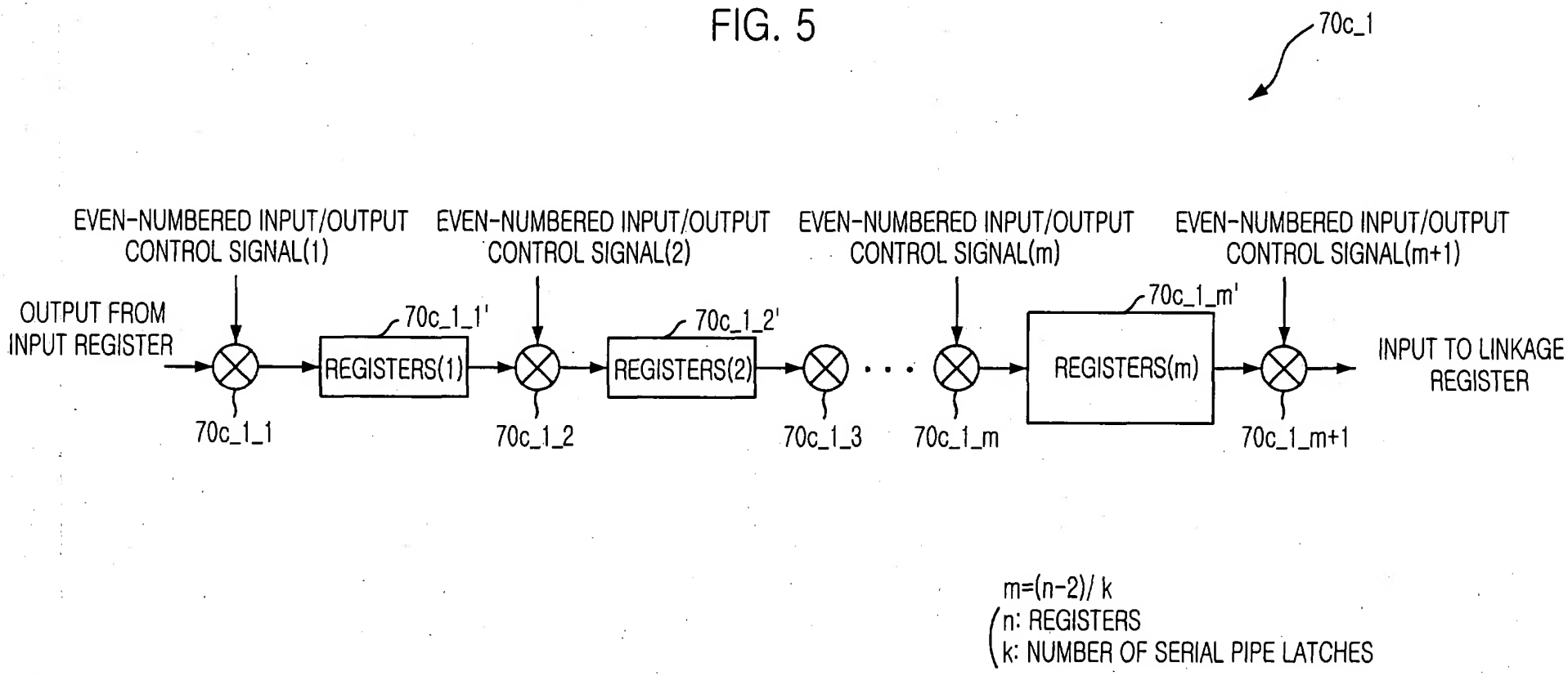

100b
EVEN-NUMBERED INPUT/OUTPUT CONTROL SIGNAL(1~n-2+k)
OUTPUT CONTROL SIGNAL
SELECTION SIGNAL
EVEN-NUMBERED DATA
70a
INPUT REGISTER
70c_1
SERIAL PIPE LATCH(1)
70c_k
SERIAL PIPE LATCH(k)
70b
LINKAGE REGISTER
80
OUTPUT MULTI-PLEXER
RISING EDGE DATA OUTPUT
ODD-NUMBERED INPUT/OUTPUT CONTROL SIGNAL(1~n-2+k)
ODD-NUMBERED DATA
70'a
INPUT REGISTER
70'c_1
SERIAL PIPE LATCH(1)
70'c_k
SERIAL PIPE LATCH(k)
70'b
LINKAGE REGISTER
FALLING EDGE DATA OUTPUT
100c
CLOCK SIGNAL
DATA OUTPUT TIMING CONTROL SIGNAL
n-2 ODD-NUMBERED INPUT/OUTPUT CONTROL SIGNAL
n-2 EVEN-NUMBERED INPUT/OUTPUT CONTROL SIGNAL
OUTPUT CONTROL SIGNAL
SELECTION SIGNAL
PIPE LATCH CIRCUIT CONTROLLER

FIG. 5



m=(n-2)/ k
(n: REGISTERS
k: NUMBER OF SERIAL PIPE LATCHES

FIG. 6

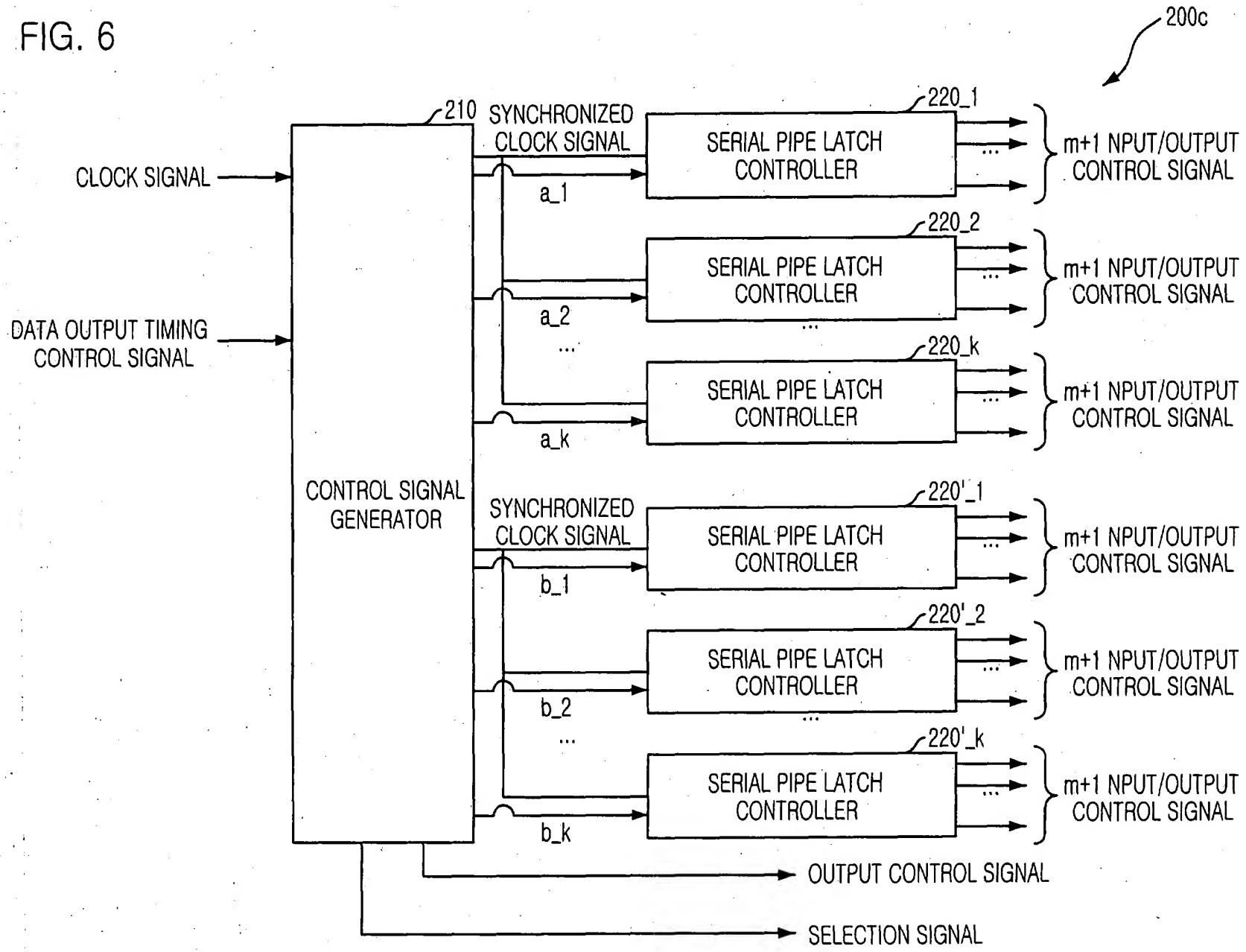

200c
210
CONTROL SIGNAL GENERATOR
CLOCK SIGNAL
DATA OUTPUT TIMING CONTROL SIGNAL
SYNCHRONIZED CLOCK SIGNAL
a_1
a_2
a_k
SYNCHRONIZED CLOCK SIGNAL
b_1
b_2
b_k
220_1
220_2
220_k
220'_1
220'_2
220'_k
SERIAL PIPE LATCH CONTROLLER
m+1 NPUT/OUTPUT CONTROL SIGNAL
OUTPUT CONTROL SIGNAL
SELECTION SIGNAL

FIG. 7

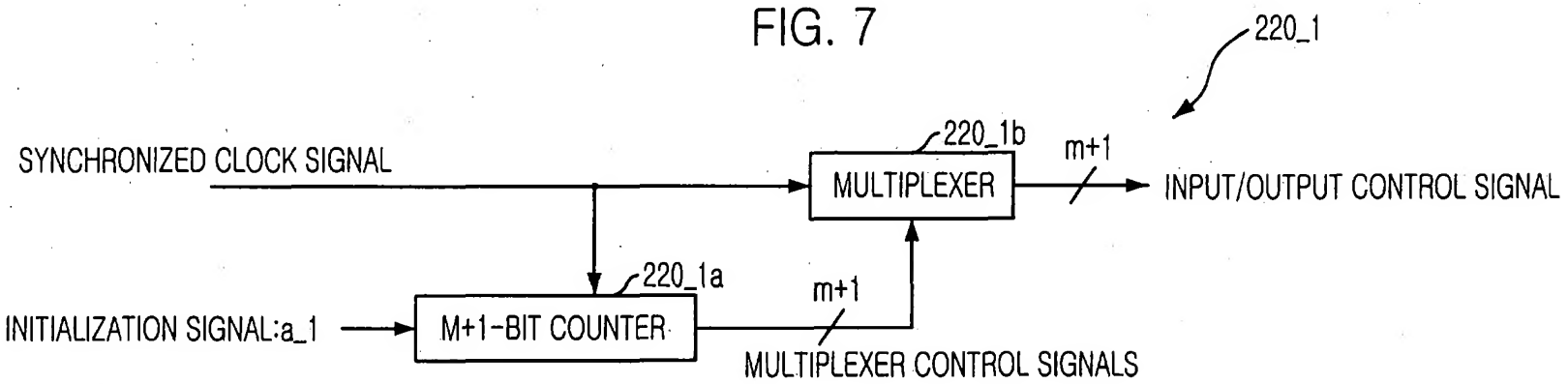

220_1
220_1b
SYNCHRONIZED CLOCK SIGNAL
MULTIPLEXER
m+1
INPUT/OUTPUT CONTROL SIGNAL
220_1a
m+1
INITIALIZATION SIGNAL:a_1
M+1-BIT COUNTER
MULTIPLEXER CONTROL SIGNALS

FIG. 8

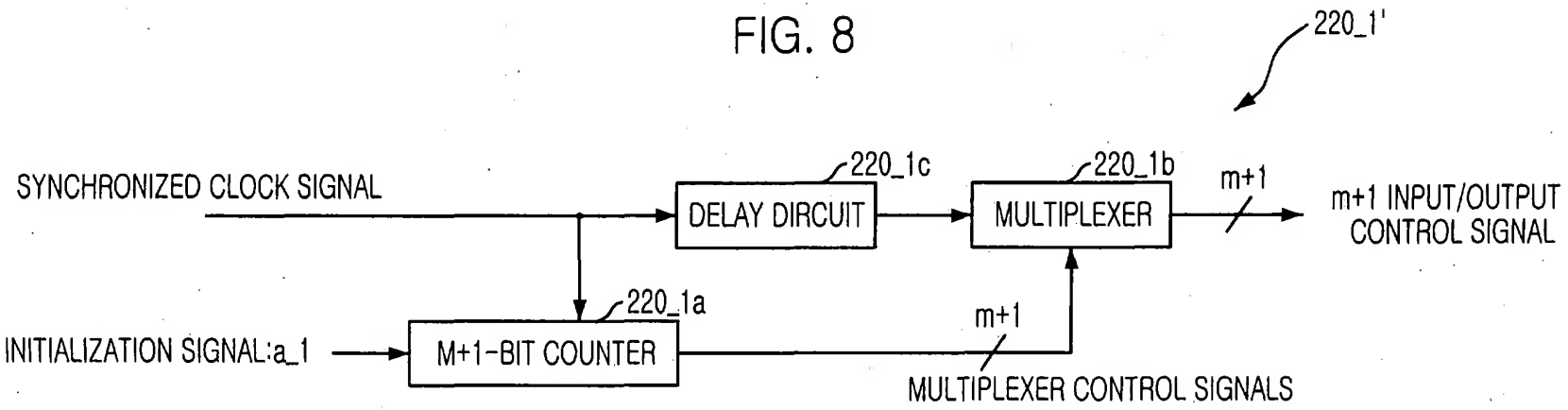

220_1'
220_1c
220_1b
SYNCHRONIZED CLOCK SIGNAL
DELAY DIRCUIT
MULTIPLEXER
m+1
m+1 INPUT/OUTPUT CONTROL SIGNAL
220_1a
m+1
INITIALIZATION SIGNAL:a_1
M+1-BIT COUNTER
MULTIPLEXER CONTROL SIGNALS

FIG. 9

	CONVENTIONAL PIPE LATCHES		PIPE LATCHES ACCORDING TO THE PRESENT INVENTION
	PARALLEL	SERIAL	
REGISTER	2n(16)	2n(16)	2n(16)
MULTIPLEXER	n(8)	1(1)	1(1)
PATH CIRCUIT	4n(32)	2n-2(14)	(2n-4)+2k(18)
TOTAL	7n(56)	4n-1(31)	(4n-3)+2k(35)
CONTROL SIGNAL	4n(40)	2n-2(16)	(2n-4)+2k(18)

FIG. 10

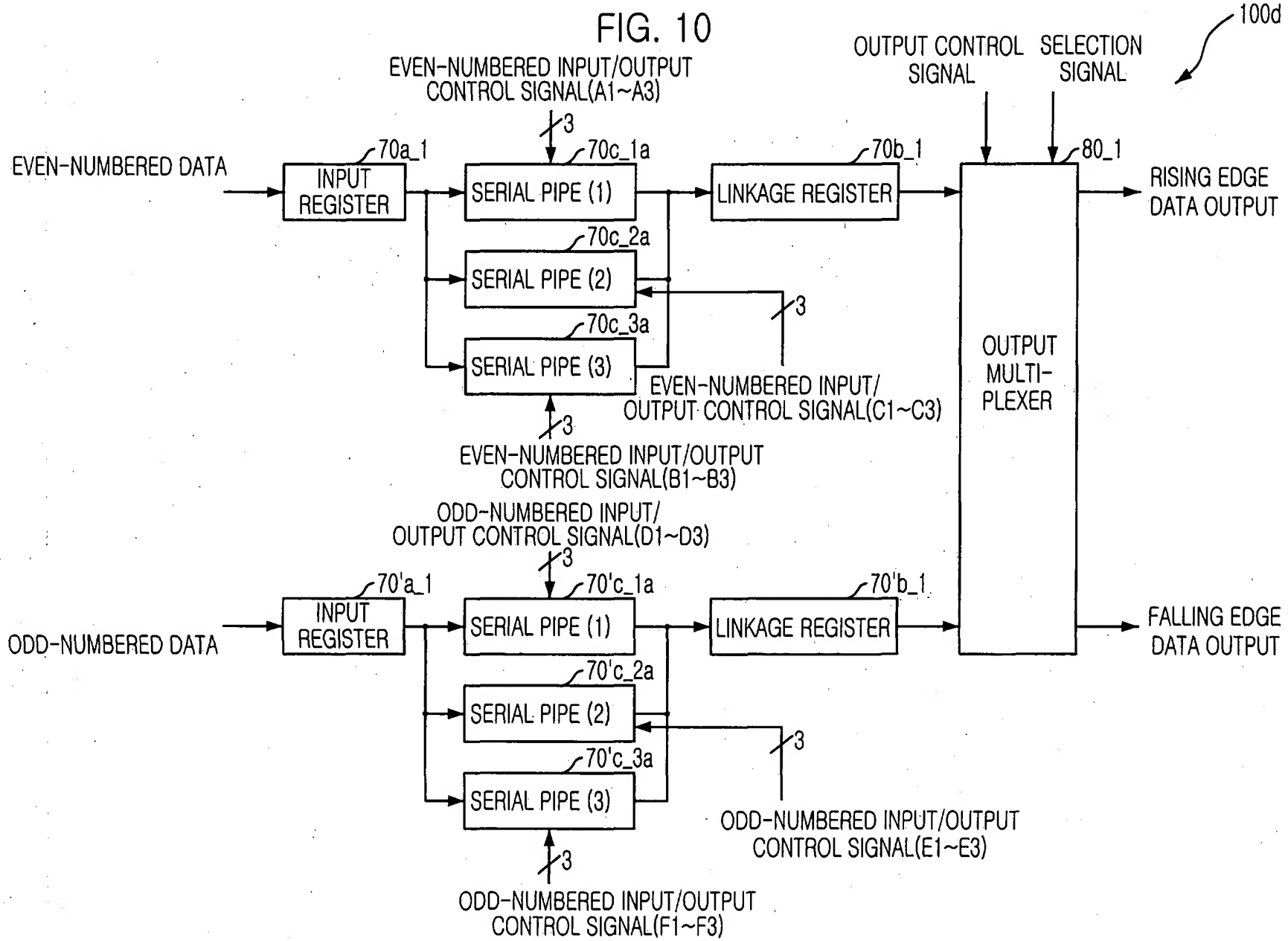

100d
OUTPUT CONTROL SIGNAL
SELECTION SIGNAL
EVEN-NUMBERED INPUT/OUTPUT CONTROL SIGNAL(A1~A3)
3
EVEN-NUMBERED DATA
70a_1
INPUT REGISTER
70c_1a
SERIAL PIPE (1)
70b_1
LINKAGE REGISTER
80_1
RISING EDGE DATA OUTPUT
70c_2a
SERIAL PIPE (2)
70c_3a
SERIAL PIPE (3)
3
EVEN-NUMBERED INPUT/ OUTPUT CONTROL SIGNAL(C1~C3)
OUTPUT MULTI-PLEXER
3
EVEN-NUMBERED INPUT/OUTPUT CONTROL SIGNAL(B1~B3)
ODD-NUMBERED INPUT/ OUTPUT CONTROL SIGNAL(D1~D3)
3
ODD-NUMBERED DATA
70'a_1
INPUT REGISTER
70'c_1a
SERIAL PIPE (1)
70'b_1
LINKAGE REGISTER
FALLING EDGE DATA OUTPUT
70'c_2a
SERIAL PIPE (2)
70'c_3a
SERIAL PIPE (3)
3
ODD-NUMBERED INPUT/OUTPUT CONTROL SIGNAL(E1~E3)
3
ODD-NUMBERED INPUT/OUTPUT CONTROL SIGNAL(F1~F3)

FIG. 11

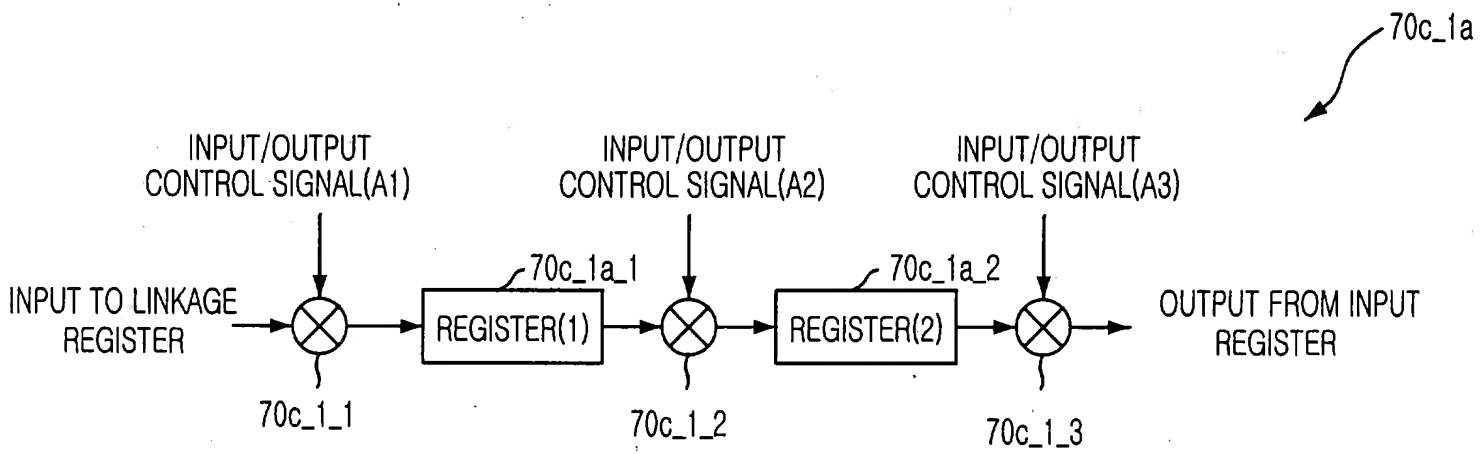

70c_1a
INPUT/OUTPUT CONTROL SIGNAL(A1)
INPUT/OUTPUT CONTROL SIGNAL(A2)
INPUT/OUTPUT CONTROL SIGNAL(A3)
INPUT TO LINKAGE REGISTER
70c_1a_1
REGISTER(1)
70c_1a_2
REGISTER(2)
OUTPUT FROM INPUT REGISTER
70c_1_1
70c_1_2
70c_1_3

FIG. 12

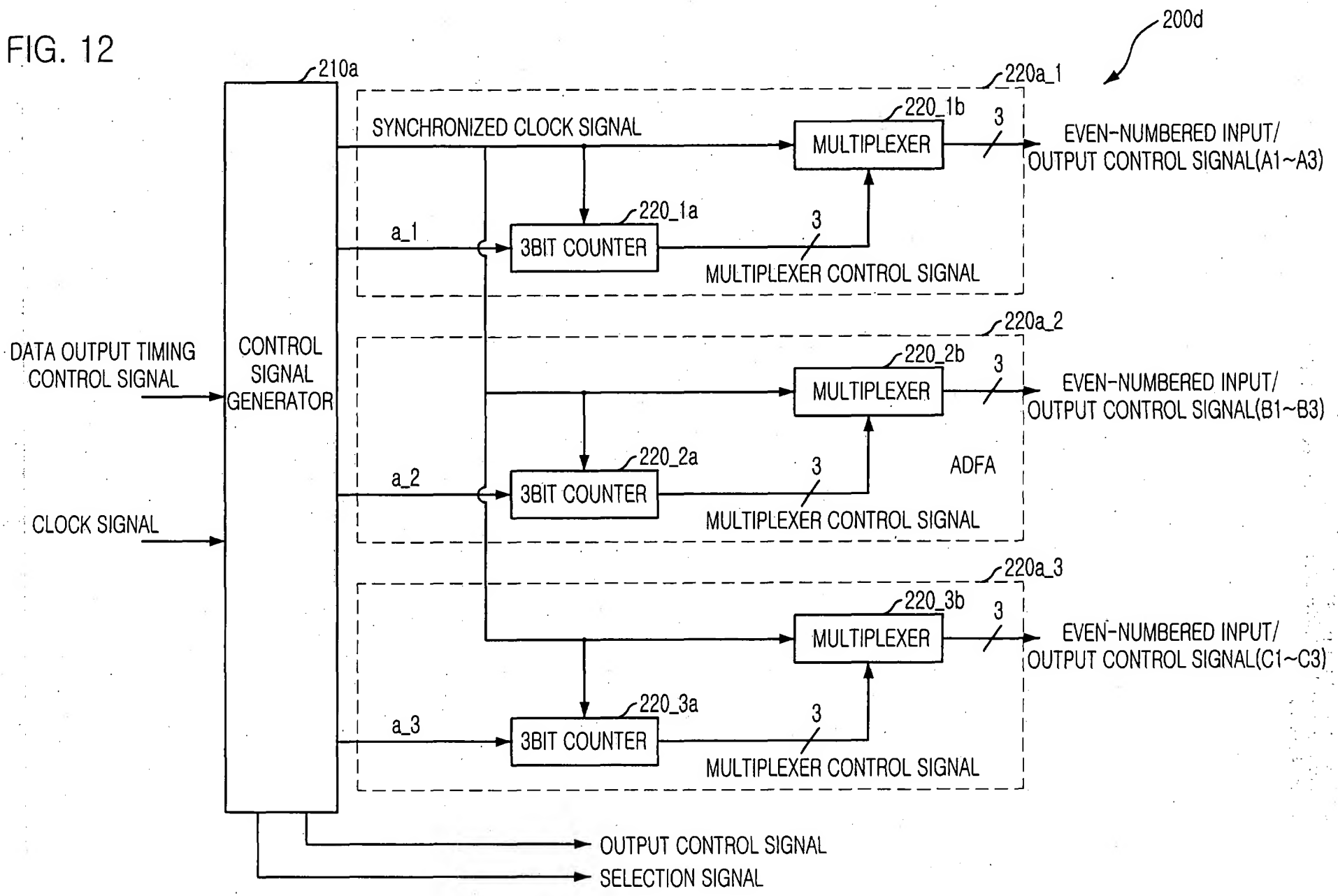

200d
210a
220a_1
220_1b
MULTIPLEXER
3
EVEN-NUMBERED INPUT/
OUTPUT CONTROL SIGNAL(A1~A3)
SYNCHRONIZED CLOCK SIGNAL
220_1a
3BIT COUNTER
a_1
3
MULTIPLEXER CONTROL SIGNAL
220a_2
220_2b
MULTIPLEXER
3
EVEN-NUMBERED INPUT/
OUTPUT CONTROL SIGNAL(B1~B3)
DATA OUTPUT TIMING
CONTROL SIGNAL
CONTROL
SIGNAL
GENERATOR
220_2a
3BIT COUNTER
a_2
3
ADFA
MULTIPLEXER CONTROL SIGNAL
CLOCK SIGNAL
220a_3
220_3b
MULTIPLEXER
3
EVEN-NUMBERED INPUT/
OUTPUT CONTROL SIGNAL(C1~C3)
220_3a
3BIT COUNTER
a_3
3
MULTIPLEXER CONTROL SIGNAL
OUTPUT CONTROL SIGNAL
SELECTION SIGNAL

FIG. 13

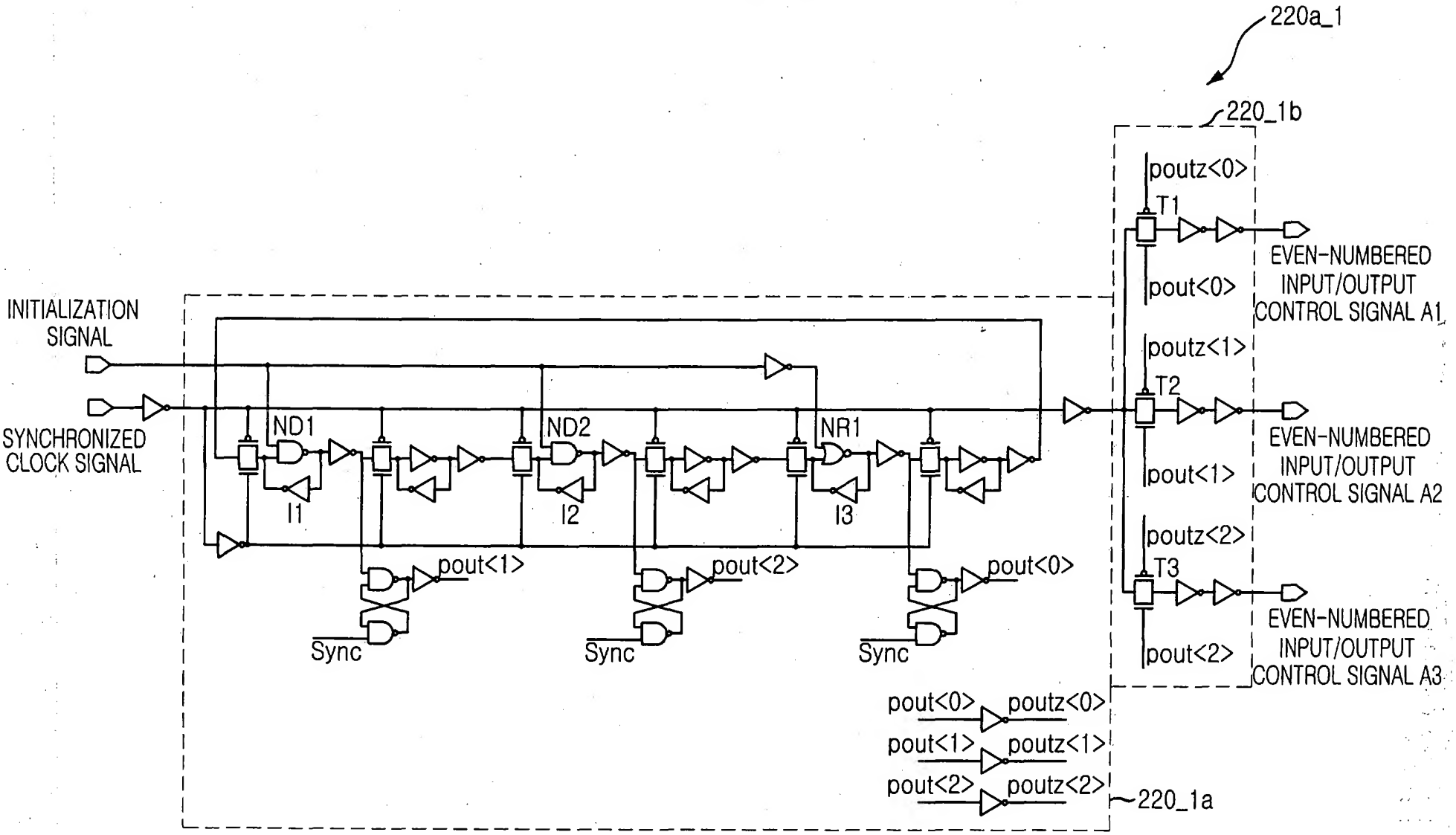

220a_1
220_1b
poutz<0>
T1
pout<0>
EVEN-NUMBERED INPUT/OUTPUT CONTROL SIGNAL A1
poutz<1>
T2
pout<1>
EVEN-NUMBERED INPUT/OUTPUT CONTROL SIGNAL A2
poutz<2>
T3
pout<2>
EVEN-NUMBERED INPUT/OUTPUT CONTROL SIGNAL A3
INITIALIZATION SIGNAL
SYNCHRONIZED CLOCK SIGNAL
ND1
ND2
NR1
I1
I2
I3
pout<1>
pout<2>
pout<0>
Sync
Sync
Sync
pout<0> poutz<0>
pout<1> poutz<1>
pout<2> poutz<2>
220_1a

FIG. 14

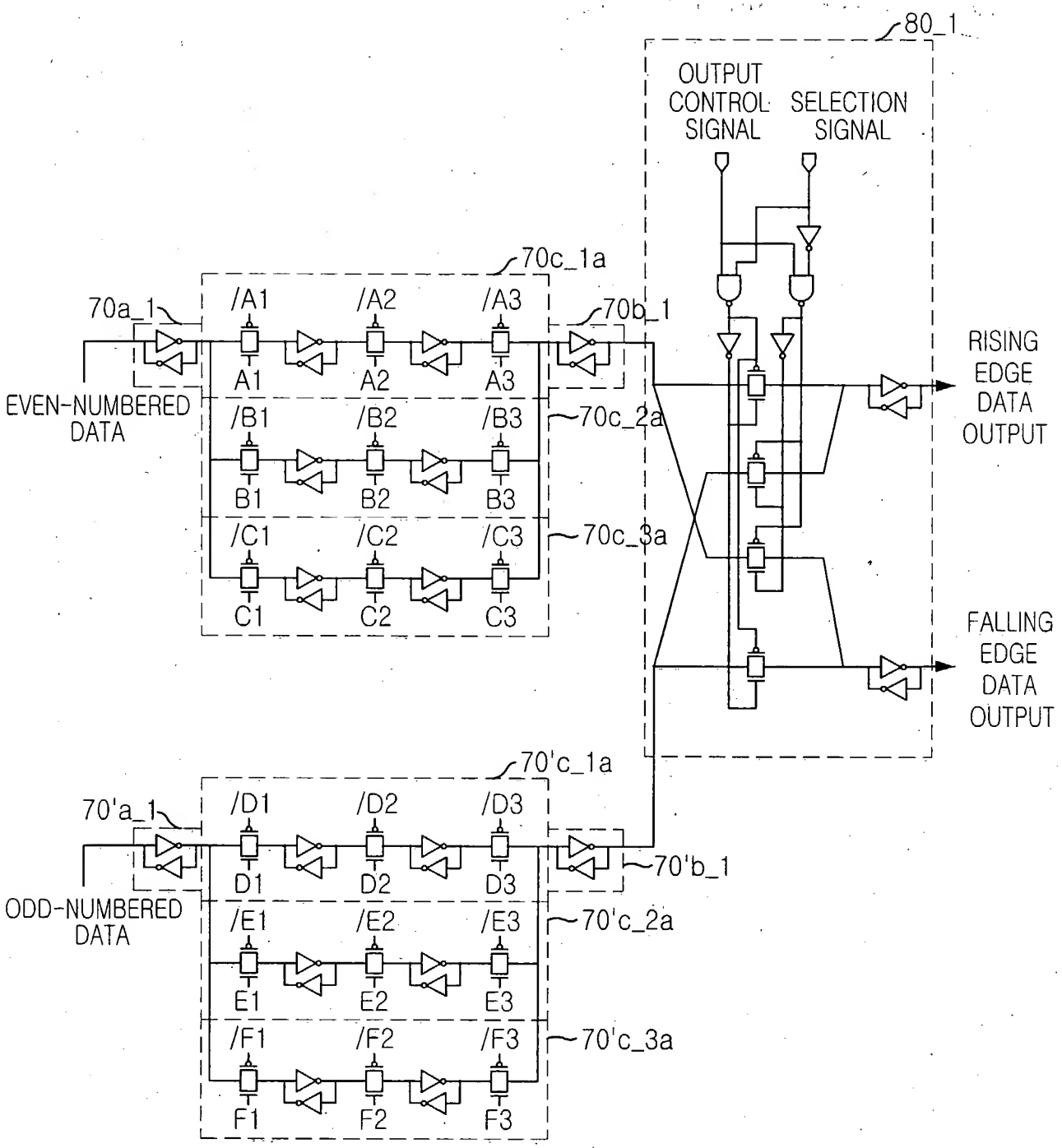
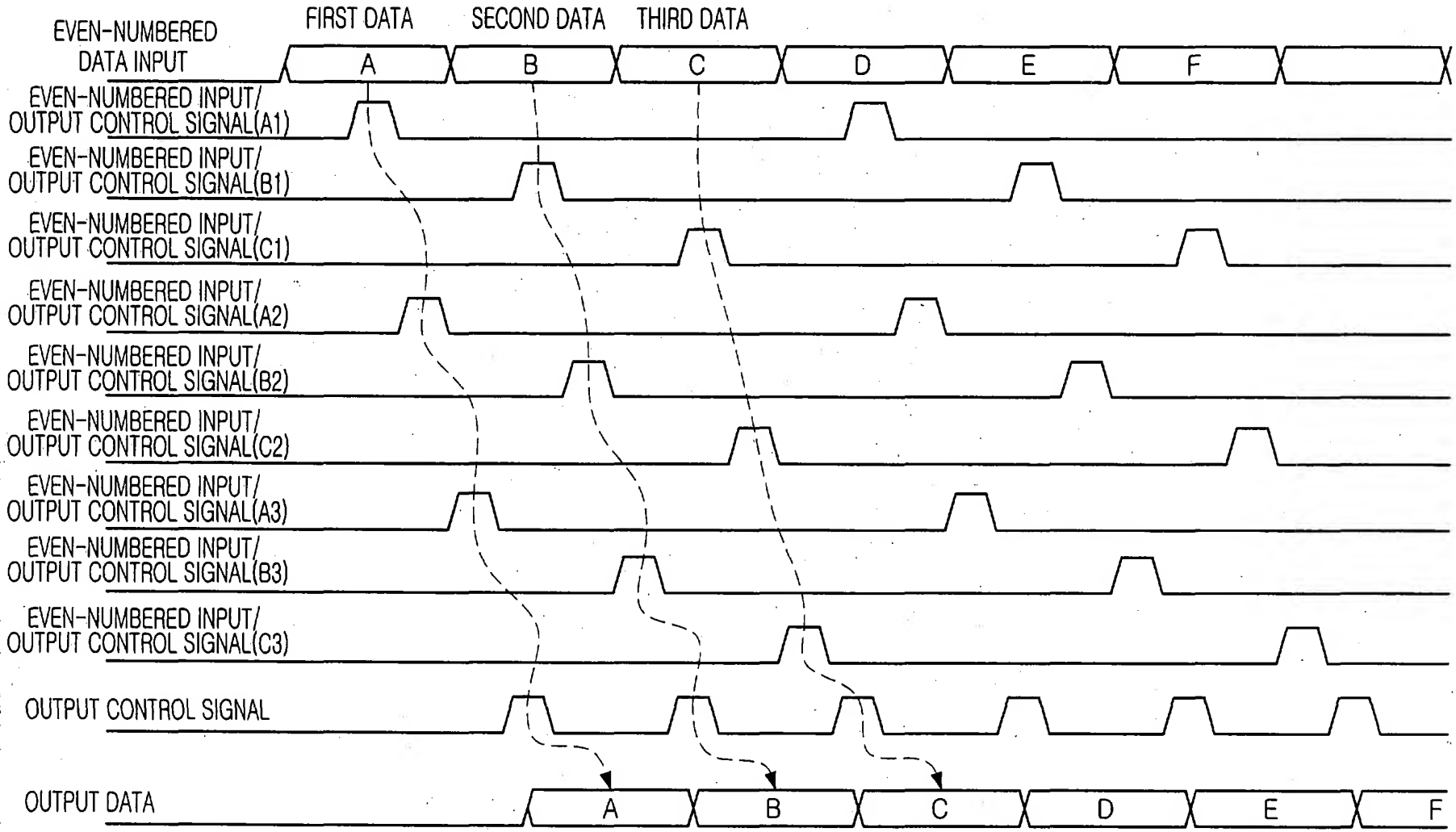

80_1
OUTPUT CONTROL SIGNAL
SELECTION SIGNAL
70c_1a
70a_1
/A1
/A2
/A3
70b_1
A1
A2
A3
EVEN-NUMBERED DATA
/B1
/B2
/B3
70c_2a
B1
B2
B3
/C1
/C2
/C3
70c_3a
C1
C2
C3
RISING EDGE DATA OUTPUT
FALLING EDGE DATA OUTPUT
70'c_1a
70'a_1
/D1
/D2
/D3
D1
D2
D3
70'b_1
ODD-NUMBERED DATA
/E1
/E2
/E3
70'c_2a
E1
E2
E3
/F1
/F2
/F3
70'c_3a
F1
F2
F3

FIG. 15


FIRST DATA
SECOND DATA
THIRD DATA
EVEN-NUMBERED DATA INPUT
A
B
C
D
E
F
EVEN-NUMBERED INPUT/ OUTPUT CONTROL SIGNAL(A1)
EVEN-NUMBERED INPUT/ OUTPUT CONTROL SIGNAL(B1)
EVEN-NUMBERED INPUT/ OUTPUT CONTROL SIGNAL(C1)
EVEN-NUMBERED INPUT/ OUTPUT CONTROL SIGNAL(A2)
EVEN-NUMBERED INPUT/ OUTPUT CONTROL SIGNAL(B2)
EVEN-NUMBERED INPUT/ OUTPUT CONTROL SIGNAL(C2)
EVEN-NUMBERED INPUT/ OUTPUT CONTROL SIGNAL(A3)
EVEN-NUMBERED INPUT/ OUTPUT CONTROL SIGNAL(B3)
EVEN-NUMBERED INPUT/ OUTPUT CONTROL SIGNAL(C3)
OUTPUT CONTROL SIGNAL
OUTPUT DATA
A
B
C
D
E
F